

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
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L2	1	((memory or semiconductor) adj chip) same selection same (criteria or rule)) and arrangement	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/18 17:57
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L5	0	((memory or semiconductor) adj chip) same (selection adj probability) same (criteria or rule))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/18 18:04
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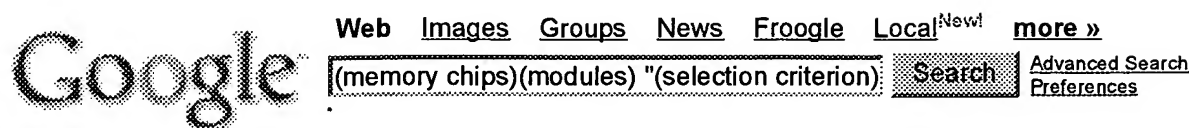
L10	188	((memory or semiconductor) adj chip) same (selection) same (buffer))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/18 18:16
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L12	163	((memory or semiconductor) adj chip) same (selection) same (storage))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/18 18:19
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S1	1265	716/8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 10:25
S2	1773	(716/1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 10:25
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S5	3	(716/1).ccls. and ((memory or semiconductor) adj chip) and modules and (data adj bus)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 10:37
S6	12	(716/4).ccls. and ((memory or semiconductor) adj chip) and modules and (data adj bus)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 10:37

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S8	1793	((memory or semiconductor) adj chip) and modules and (data adj bus)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 10:38
S9	218	((memory or semiconductor) adj chip) same modules) and selected and (data adj bus)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 11:19
S10	29	((memory or semiconductor) adj chip) same (group or set) same modules) and selected and (data adj bus)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 11:22
S11	16	((memory or semiconductor) adj chip) same (group or set) same (memory adj modules)) and selected and (data adj bus)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 12:15
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S15	5	(365/63).ccls. and (((memory or semiconductor) adj chip) same (group or set) same (memory adj modules)) and selected and (data adj bus)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 12:16
S16	4	(365/51).ccls. and (((memory or semiconductor) adj chip) same (group or set) same (memory adj modules)) and selected and (data adj bus)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 12:16

S17	1	(365/52).ccls. and (((memory or semiconductor) adj chip) same (group or set) same (memory adj modules)) and selected and (data adj bus)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 12:33
S18	0	(((memory or semiconductor) adj chip) same (group or set) same (memory adj modules)) and selected and (data adj bus) and statistical	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 12:36
S19	0	(((memory or semiconductor) adj chip) same (group or set) same (memory adj modules)) and selected and (data adj bus) and (statistic\$ or probabil\$)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 12:38
S20	33	(((memory or semiconductor) adj chip) same modules same select) and (data adj bus)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 18:38
S21	18	(((memory or semiconductor) adj chip) same modules same select) and (data adj bus) and cycle	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 18:40
S22	3	(((memory or semiconductor) adj chip) same modules same select) and (data adj bus) and (two adj cycles)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 18:44
S23	493	((memory or semiconductor) adj chip) and (data adj bus) and (two adj cycles)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 18:45
S24	7	(((memory or semiconductor) adj chip) same modules) and (data adj bus) and (two adj cycles)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 18:46
S25	1804	((memory or semiconductor) adj chip) same selection	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/18 10:04
S26	32	(((memory or semiconductor) adj chip) same selection) same modules	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/18 10:10

S27	0	((memory or semiconductor) adj chip) adj selection) same modules	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/18 10:06
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S33	30	(memory adj chip) same (two adj cycles)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/18 12:03
S34	719	((memory or semiconductor) adj chip) and (selection same (temperature or statistical))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/18 12:06
S35	43	((memory or semiconductor) adj chip) same (selection same (temperature or statistical))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/18 12:20
S36	7	((memory or semiconductor) adj chip) same (selection adj (criteria or rule))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/18 12:58

S37	15	((memory or semiconductor) adj chip) same selection same (criteria or rule)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/18 17:55
S38	0	((memory or semiconductor) adj chip) adj grouping) same (criteria or rule)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/18 13:48
S39	1	(memory adj chips) and ((chip adj selection) same (criteria or rule))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/18 13:48
S40	0	((memory or semiconductor) adj chip) same selection same activation same (criteria or rule)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/18 13:57
S41	36	((memory or semiconductor) adj chip) same selection same activation	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/18 13:57
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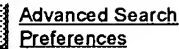
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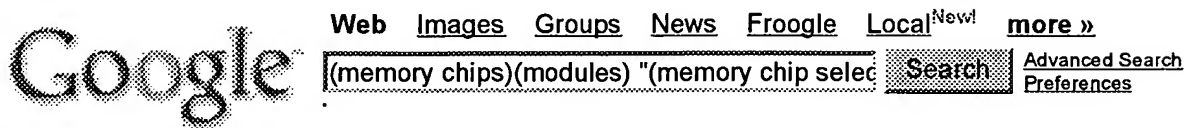
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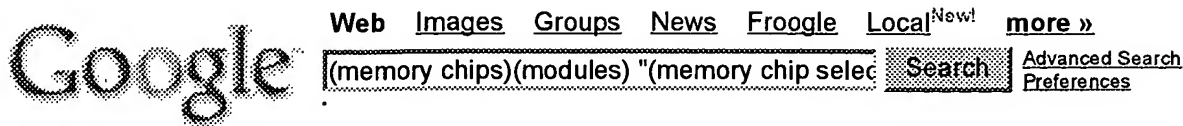
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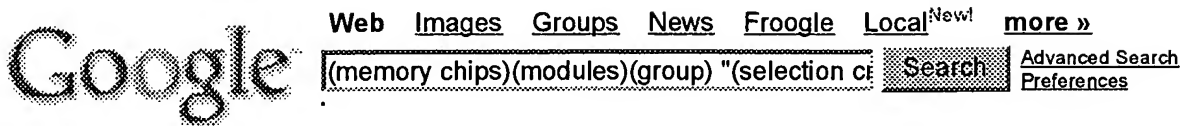
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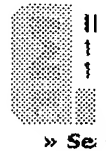
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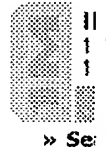
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1 Fabrication process for Josephson computer ETL-JC1 using Nb tunnel junctions

Nakagawa, H.; Kurosawa, I.; Aoyagi, M.; Takada, S.;

Magnetics, IEEE Transactions on , Volume: 27 , Issue: 2 , Mar 1991

Pages:3109 - 3112

[\[Abstract\]](#) [\[PDF Full-Text \(696 KB\)\]](#) **IEEE JNL**

2 Bidirectionally propagating fast access bubble memory chips

Morimoto, A.; Urai, H.; Yoshimi, K.; Fujiwara, S.;

Magnetics, IEEE Transactions on , Volume: 15 , Issue: 6 , Nov 1979

Pages:1712 - 1714

[\[Abstract\]](#) [\[PDF Full-Text \(520 KB\)\]](#) **IEEE JNL**

3 Effects of N-H₂doses in ion-implanted bubble memory test chips

Nelson, T.; Ballantine, J.; Reith, L.; Roman, B.; Slusky, S.; Wolfe, R.;

Magnetics, IEEE Transactions on , Volume: 18 , Issue: 6 , Nov 1982

Pages:1358 - 1360

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4 Design and characteristics of 4Mb hybrid bubble memory chips

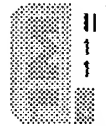
Fedeli, J.; Magnin, J.;

Magnetics, IEEE Transactions on , Volume: 22 , Issue: 5 , Sep 1986

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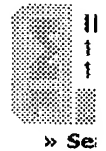
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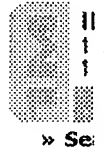
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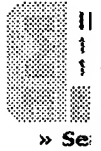
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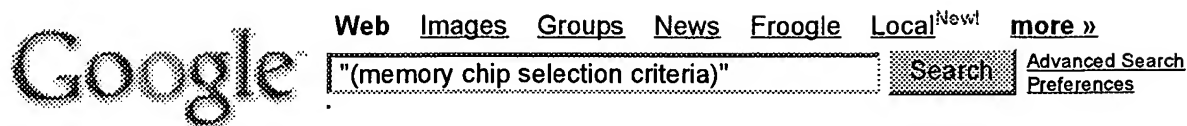
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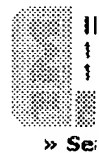
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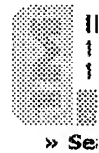
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Solid-State Circuits, IEEE Journal of , Volume: 4 , Issue: 5 , Oct 1969

Pages:295 - 296

[\[Abstract\]](#)[\[PDF Full-Text \(400 KB\)\]](#)**IEEE JNL****2 Scalable IP lookup for Internet routers***Taylor, D.E.; Turner, J.S.; Lockwood, J.W.; Sproull, T.S.; Parlour, D.B.;*

Selected Areas in Communications, IEEE Journal on , Volume: 21 , Issue: 4 , 2003

Pages:522 - 534

[\[Abstract\]](#)[\[PDF Full-Text \(960 KB\)\]](#)**IEEE JNL****3 The design of a one megabit non-volatile M-R memory chip using 1.1 μm cells***Pohm, A.V.; Huang, J.S.T.; Daughton, J.M.; Krahn, D.R.; Mehra, V.;*

Magnetics, IEEE Transactions on , Volume: 24 , Issue: 6 , Nov 1988

Pages:3117 - 3119

[\[Abstract\]](#)[\[PDF Full-Text \(200 KB\)\]](#)**IEEE JNL****4 A 16Kb static MTL/I²L memory chip***Wiedmann, S.; Heuber, K.; Klein, W.;*

Solid-State Circuits Conference. Digest of Technical Papers. 1980 IEEE International , Volume: XXIII , Feb 1980

Pages:222 - 223